REMARKS

This Amendment After Final Rejection is submitted in response to the outstanding final Office Action, dated March 1, 2006. The present application was filed on January 5, 2004 with claims 1 through 42. Claims 38-42 were cancelled in the Amendment and Response to Office Action dated December 13, 2005. Claims 1 through 37 are presently pending in the above-identified patent application. Claims 1, 3, 4, 6, 16, 21, 22, and 24 are proposed to be amended herein.

This amendment is submitted pursuant to 37 CFR §1.116 and should be entered. The Amendment places all of the pending claims, i.e., claims 1 through 37, in a form that is believed allowable, and, in any event, in a better form for appeal. It is believed that examination of the pending claims as amended, which are consistent with the previous record herein, will not place any substantial burden on the Examiner. In any case, a Request for Continued Examination is being submitted herewith.

In the Office Action, the Examiner has requested that a prior art label be added to Figures 1B, 2B, 4B, 5B, and 6-9. The Examiner has objected to the formal drawings, and requested that they be labeled as "Replacement Sheets." With regard to claim 22, the Examiner asserts that the Drawings do not show an electrical connection between the control line and signal line. Claims 1-2, 9-10, 13-15, 21, 23, 31 and 35 were rejected under 35 USC 102(b) as being anticipated by Mead et al. (United States Patent No. 5,844,265). The Examiner objected to claims 3-8, 11-12, 16-20, 22, 24-30, 32-34 and 36-37 as being dependent on a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Formal Objections

Drawings

The Examiner has requested that a prior art label be added to FIGS. 1B, 2B, 4B, 5B, and 6-9. The Examiner has objected to the formal drawings, and requested that they be labeled as "Replacement Sheets." Applicants submit that FIGS. 1A, 1B, 1C, 4A, 4B, 6 and 8 show a gated diode structure with only a gate and a source (and no drain). There are only two terminal areas for the gated diode. The present invention recognizes that this

structure without the drain leads to significantly smaller gated diode physical structure (which keeps the area much smaller in applications such as memories and sense amplifiers). Thus, FIGS. 1A, 1B, 1C, 4A, 4B, 6 and 8 are different from what is shown by the prior art, including Mead.

In the Amendment and Response to Office Action dated December 13, 2005, Applicants labeled FIGS. 2B, 5B, 7 and 9 as "prior art" in accordance with the Examiner's suggestion and each sheet was labeled as a "Replacement Sheet."

Applicants respectfully request that the objection to the drawings be withdrawn.

Claim 22

With regard to claim 22, the Examiner asserts that the Drawings do not show an electrical connection between the control line and signal line. Applicants submit that the configuration of claim 22 does not require an electrical connection between the control line and signal line.

Claim 22 is directed to a basic method of operation of the gated diode amplifier, and how to modify the voltage of the control line. Claim 22 requires that a sensed voltage is determined based on a voltage at the output, whereby the sensed voltage will be amplified when a voltage on the first terminal relative to the second terminal is above the threshold voltage and will not be amplified when a voltage on the first terminal relative to the second terminal is below the threshold voltage. Support for claim 22 can be found in the original specification, for example, in Figs. 11A, 11B, 11C, 12A, 12B, 14 and 16 and the corresponding text.

As the Examiner has pointed out, the sensed voltage is necessarily the same as the voltage on the signal line.

For an n-type gated diode, the first terminal is the gate (claim 21), and the second terminal is the source (claim 21); thus, the "voltage of the first terminal relative to the second terminal" is Vgs.

If Vgs > Vthreshold (or Vt or Vt_gd as denoted in the description), the gated diode stores charges in the inversion layer and has a large capacitance Cgs; when the voltage

Vs of the second terminal (i.e., the source coupled to the control line) is modified (as required by claim 21) (by raising from low to high, say VB), the voltage at the first terminal (Vg) will be raised to Vout(1) = VB*Rc/(1+Rc)+VL_HIGH, as shown also in FIG. 12A.

If Vgs < Vthreshold (or Vt or Vt_gd as denoted in the description), the gated diode stores very little charge and has a very small capacitance Cgs; when the voltage Vs of the second terminal (i.e., the source coupled to the control line) is modified (as required by claim 21) (by raising from low to high, say VB), the voltage at the first terminal (Vg) will be raised only slightly to Vout(0) = VB*rc/(1+rc)+VL_LOW, as shown in FIG. 12A.

As defined in the description, Rc >> rc (e.g., Rc = 10, rc = 0.1), and dVin = VL_HIGH - VL_LOW (typically VL_LOW ~ 0). The difference between the two cases determines the gain of the signal amplification, wherein the gain equals (Vout(1) - Vout(0)) / (VB_HIGH - 0), and is typically greater than 1.

Thus, Applicants respectfully request withdrawal of the formal objections.

Claims 3 and 24

The Examiner objected to claims 3-8, 11-12, 16-20, 22, 24-30, 32-34 and 36-37 as being dependent on a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3 and 24 have been amended to include all of the limitations of their base claim and any intervening claims. Thus, claims 3-8, 17-20, 24-28, and 36-37 should now be allowable and Applicants respectfully request that the rejections of the cited claims be withdrawn.

Claims 1, 3, 4, 6, 16, 21, 22 and 24

Claims 1, 3, 4, 6, 16, 21, 22, and 24 have been amended to require first, second, third, and fourth voltage ranges. This amendment was required to make claims 1 and 21 consistent with claims 14-15, for example. Support for this amendment can be found in original claims 1 and 21.

Prior Art Rejections

Claims 1-2, 9-10, 13-15, 21, 23, 31 and 35 were rejected under 35 USC 102(b) as being anticipated by Mead et al. The Examiner asserts that:

> Mead discloses a circuit 10 for amplifying signals. The circuit 10 comprises a control line (LOAD BIAS connected to a bias voltage source); and
>
> a two terminal semiconductor device 62-1 (MOS transistor used as varactor with source and drain short-circuited), having first and second terminals, the first terminal (gate of varactor 62-2) coupled to a signal line 194-1 (of sense amplifier 10), and the second terminal coupled to the control line (capacitively, through 16-1), where the two terminal semiconductor device is adapted ....

Initially, it is noted that the varactors (62-n) of Mead are not even used for signal amplification. Rather, Mead teaches that the "(u)se of a varactor structure allows compression of the output signal over a wide dynamic range of input signals." (See, col. 3, lines 25 – 26.) The Examiner is asserting that the three terminal MOS transistors 62-1 through 62-4 in FIG. 7 of Mead are two terminal devices, because the source and drain of the transistors 62-n are short circuited. Assuming for the sake of argument that the transistors 62-1 through 62-4 with connected source and drain are two terminal devices, Mead still does not teach at least one a number of other limitations of the independent claims. The present invention does not claim a two-terminal structure by itself. Rather, each independent claim explicitly recites connecting such two-terminal devices in a certain way to perform signal amplification.

The transistors 62-n of FIG. 7, such as transistor 62-1, are connected between a LOAD BIAS (the Examiner is calling this the control line) and first sense line 194-1 (the Examiner is calling this the signal line).

First, the transistors 62-n in FIG. 7 are not directly connected to the LOAD BIAS, but rather are connected to the LOAD BIAS via the output signal (not numbered in FIG. 7 of Mead, but numbered as OUT or 28 in FIG. 1 of Mead). It is noted that the LOAD BIAS is a DC voltage to bias the amplifier which comprises the transistors 12, 14 and 16 in FIG. 1 (often referred to as a cascode amplifer).

Both independent claims 1 and 21 require that "the second terminal (is) coupled to the control line." Assuming, for the sake of argument, that one even considers the LOAD BIAS as a control line, the varactors (62-n) are not coupled to a control line. Indeed, it is coupled or directly connected to the output of the amplifier which is clearly a signal, numbered as OUT or 28 in FIG. 1 of Mead). Further, in column 3, lines 23 - 25 of Mead, it is noted that "... a varactor may be connected between the input and output of amplifier." The input and output of an amplifier are signals, which cannot be considered as a control line.

Applicants also note that Mead teaches that

> the drain of cascode transistor 14 is connected to the drain of load transistor 16. The source of load transistor 16 is connected to ground rail 24 and the gate of load transistor 16 is connected to load bias node 26. *Load bias node 26 is connected to a bias voltage source* ***supplying a load bias voltage well above the threshold voltage*** *of the transistor.* The output node 28 of amplifier 10 is the common connection of the drains of cascode transistor 14 and load transistor 16.
> (Col. 3, lines 10-18; emphasis added.)

Claims 1 and 21 have been amended to require wherein the two terminal semiconductor device is ***adapted to amplify said signal*** *in response to a* ***substantial change*** *in voltage of said control signal.* As noted above, Mead does ***not*** disclose or suggest that the varactor is *adapted to amplify a signal*, and does ***not*** disclose or suggest a *substantial change in voltage of a control signal.*

Thus, Mead does ***not*** disclose or suggest that "the second terminal (is) coupled to the control line" and does ***not*** disclose or suggest "wherein the two terminal semiconductor device is adapted to amplify said signal in response to a substantial change in voltage of said control signal," as required by independent claims 1 and 21, as amended.

Applicants respectfully request that the rejection under section 102 be withdrawn.

Dependent Claims

The Examiner has already indicated that claims 3-8, 11-12, 16-20, 22, 24-30, 32-34 and 36-37 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The remaining dependent claims are dependent on independent claims 1 and 21, and are therefore patentably distinguished over Mead because of their dependency from amended independent claims 1 and 21 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims following entry of the amendments, i.e., claims 1-37, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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